

Fig. 1

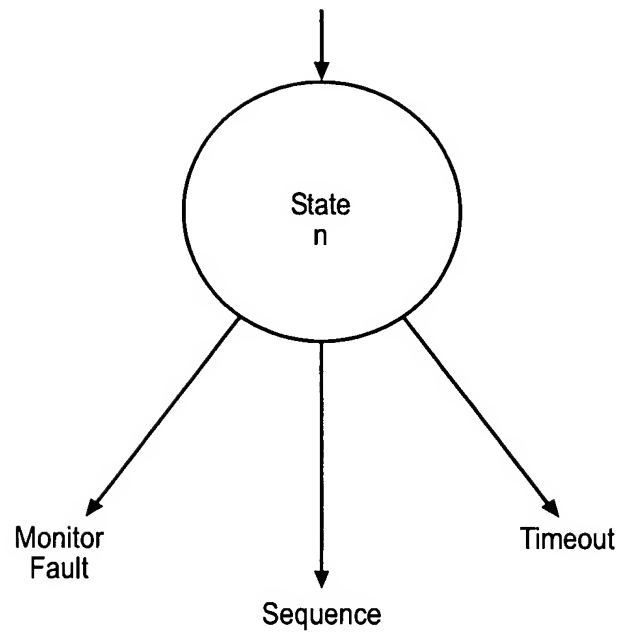


Fig. 2

| PDO Outputs  | IDLE1 | IDLE2 | EN3V3 | EN2V5 | DIS3V3 | DIS2V5 | PWRGD | FSEL1 | FSEL2 |
|--------------|-------|-------|-------|-------|--------|--------|-------|-------|-------|
| PDO1 = 3V3ON | 0     | 0     | 1     | 1     | 0      | 1      | 1     | 1     | 1     |
| PDO2 = 2V5ON | 0     | 0     | 0     | 1     | 0      | 0      | 1     | 1     | 1     |
| PDO3 = Fault | 0     | 0     | 0     | 0     | 1      | 1      | 0     | 1     | 1     |

Fig. 10

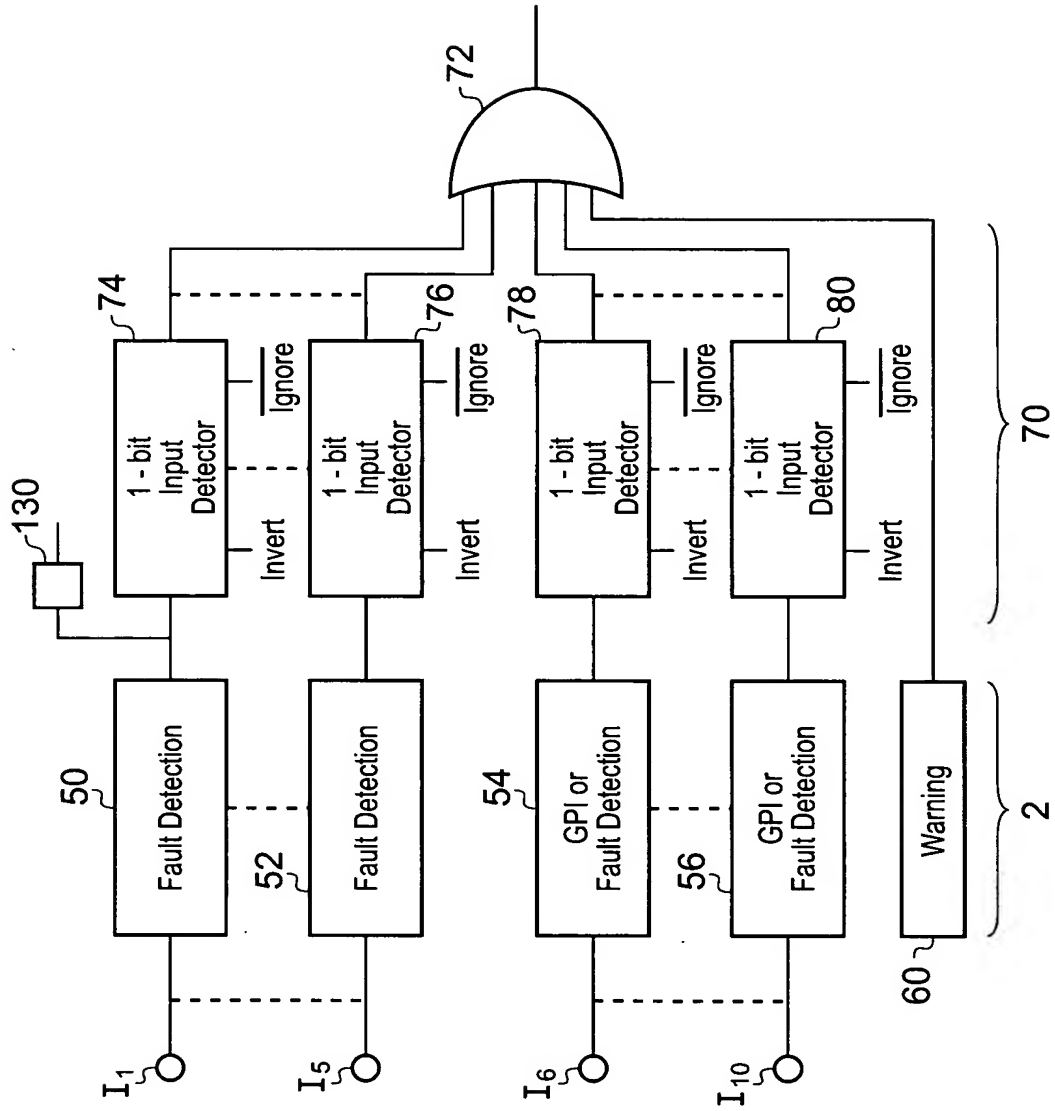


Fig. 3

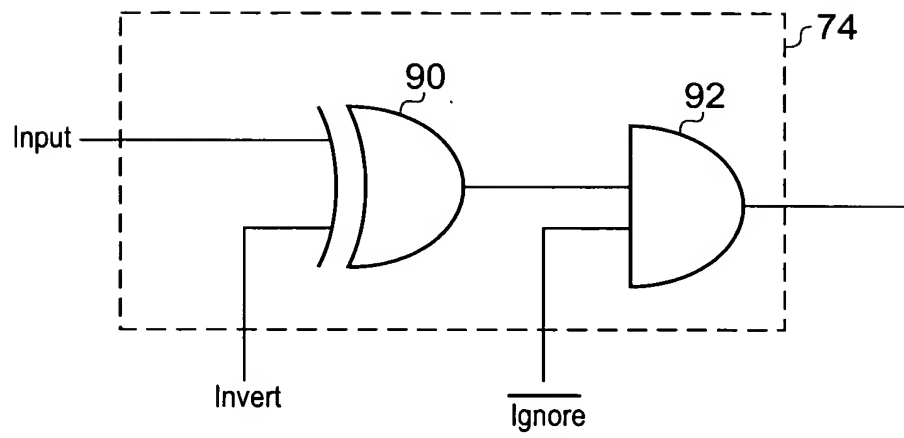


Fig. 4

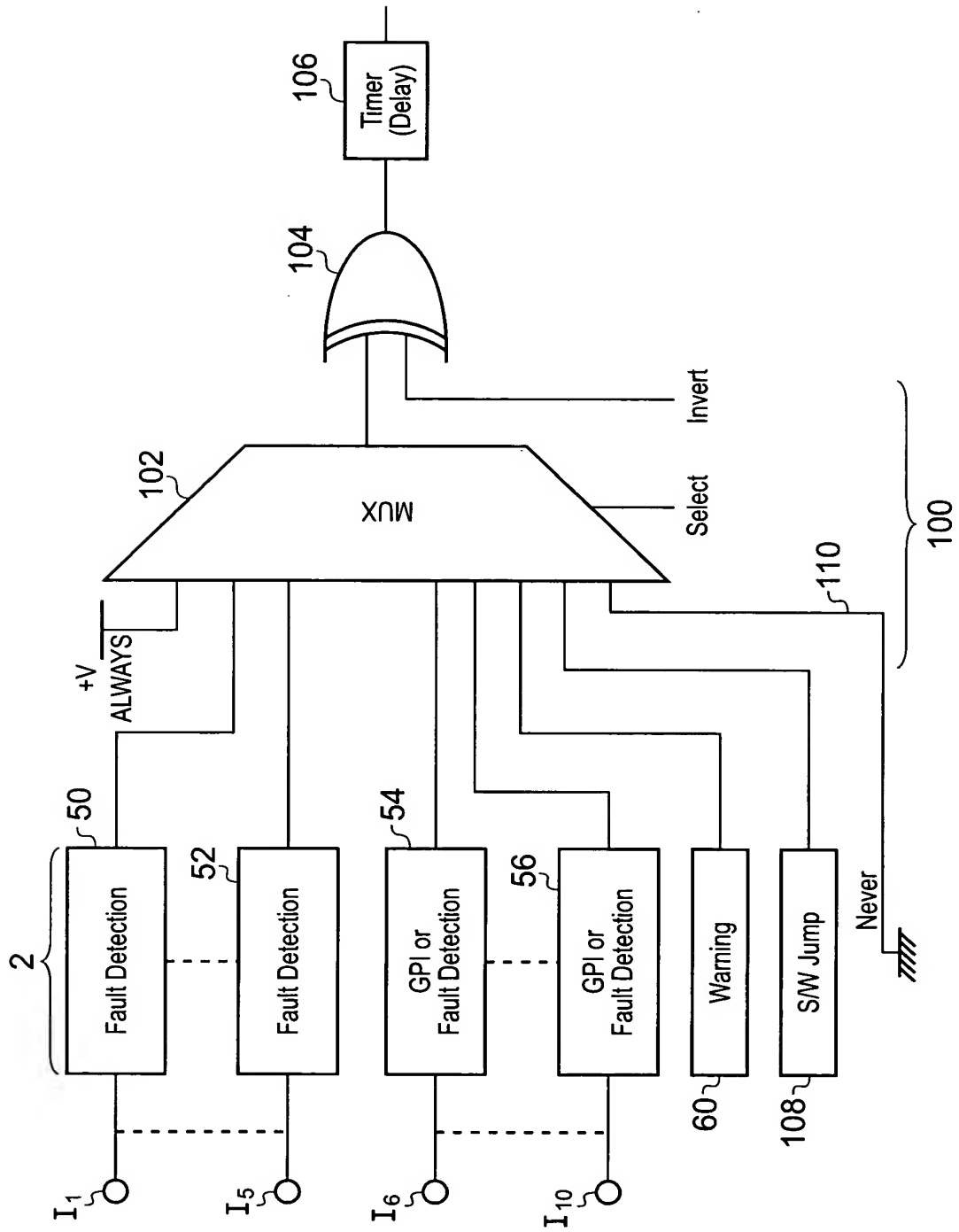


Fig. 5

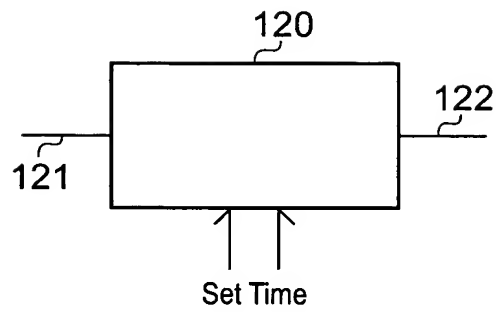


Fig. 6

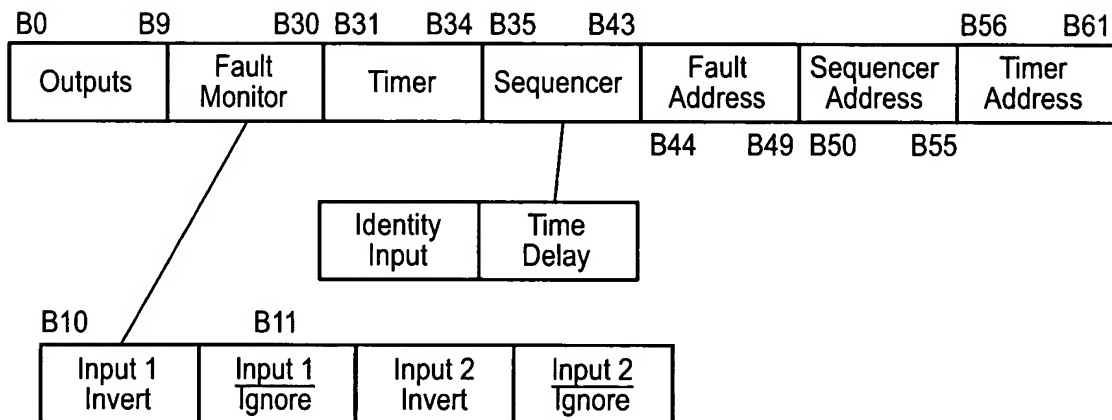


Fig. 7

| State  | End of Step                                | Timeout   | Monitor   |
|--------|--|---|---|
| IDLE1  | If VX1 is LOW then<br>goto State IDLE2     |   |   |
| IDLE2  | If VP1 is OK then<br>goto State EN3V3      |   |   |
| EN3V3  | If VP2 is OK then<br>goto State EN2V5      | If VP2 is NOT OK after<br>10ms then goto State DIS3V3 | If VP1 is NOT OK<br>then goto State IDLE1               |
| DIS3V3 | If VX1 is HIGH then<br>goto State IDLE1    |   |   |
| EN2V5  | If VP3 is OK then<br>goto State PWRGD      | If VP3 is NOT OK after<br>20ms then goto State DIS2V5 | If VP1 or VP2 is NOT OK<br>then goto State FSEL2        |
| DIS2V5 | If VX1 is HIGH then<br>goto State DIS3V3   |   |   |
| FSEL1  | If VP3 is NOT OK then<br>goto State DIS2V5 |   | If VP1 or VP2 is NOT OK<br>then goto State FSEL2        |
| FSEL2  | If VP2 is NOT OK then<br>goto State DIS3V3 |   | If VP1 is NOT OK<br>then goto State IDLE1               |
| PWRGD  | If VX1 is HIGH then<br>goto State DIS2V5   |   | If VP1 or VP2 or VP3 is NOT OK<br>then goto State FSEL1 |

Fig. 8

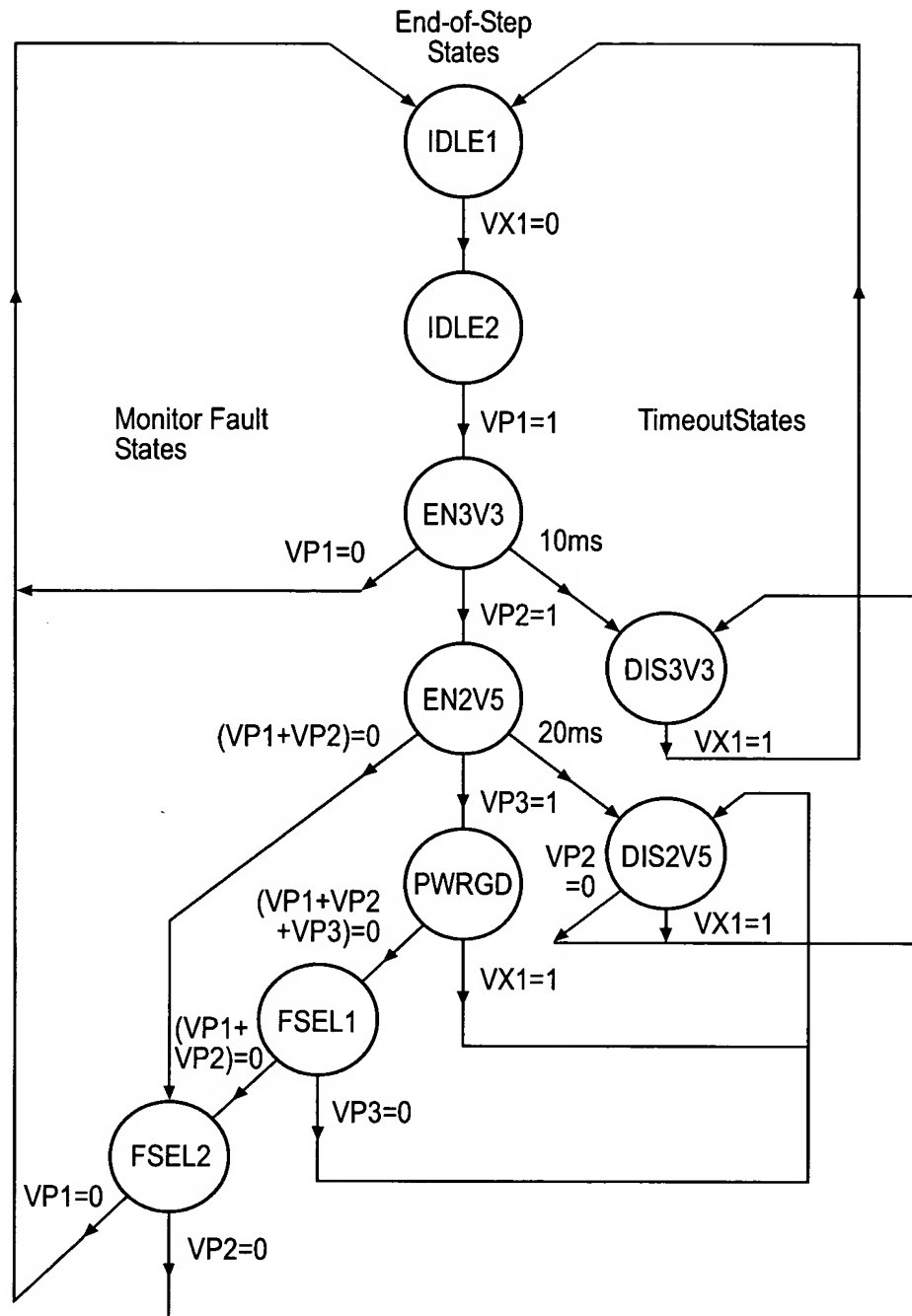


Fig. 9